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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 :		(11) International Publication Number:	WO 92/06424
G05F 3/24	A1	(43) International Publication Date:	16 April 1992 (16.04.92)

(21) International Application Number: PCT/US91/06939

(22) International Filing Date: 24 September 1991 (24.09.91)

(30) Priority data:
590,655 28 September 1990 (28.09.90) US

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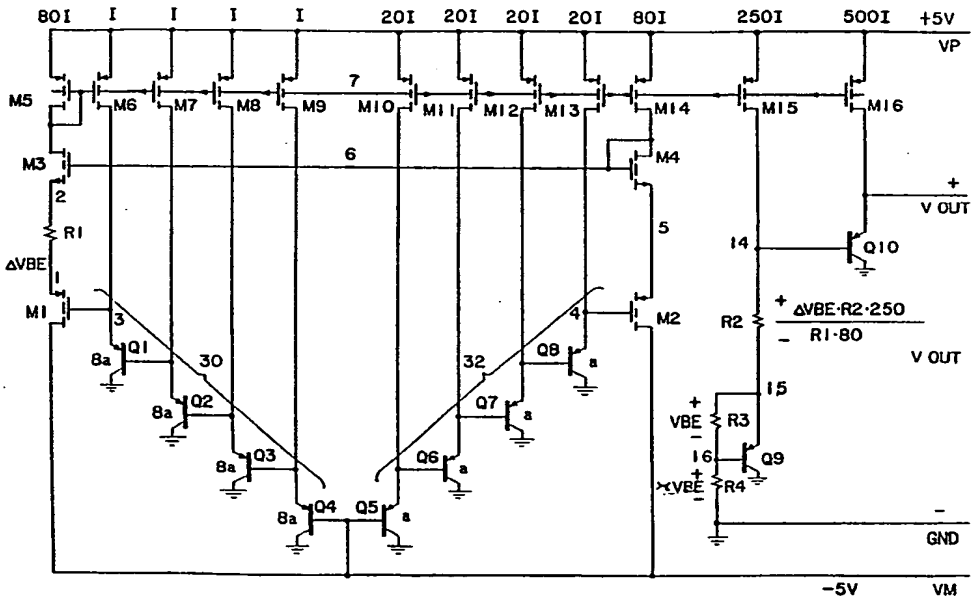
(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), DK (European patent), ES (European patent), FR (European patent), GB (European patent), GR (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent).

Published
With international search report.
With amended claims.

(54) Title: CMOS VOLTAGE REFERENCE WITH STACKED BASE-TO-EMITTER VOLTAGES



(57) Abstract

A band-gap voltage reference forming part of a CMOS IC chip. A ΔV_{BE} voltage is developed by stacked pairs of parasitic bipolar transistors (Q1, Q8; Q2, Q7; Q3, Q6; Q4; Q5), with the transistors (Q1-Q8) of each pair operated at different current densities. MOS buffer transistors (M1-M4) are connected at corresponding ends of the stacks where the ΔV_{BE} voltage is developed. The bipolar transistors are driven by MOS current sources (M6-M13).

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CMOS VOLTAGE REFERENCE WITH STACKED BASE-TO-EMITTER VOLTAGES

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to voltage reference circuits of the band-gap type. More particularly, this invention relates to band-gap circuits suited for use with CMOS integrated-circuit (IC) chips.

2. Description of the Prior Art

Band-gap voltage regulators have been used for a number of years for developing reference voltages which remain substantially constant in the face of temperature variations. Such circuits generally develop a voltage proportional to the difference between base-to-emitter voltages (ΔV_{BE}) of two transistors operated at different current densities. This voltage will have a positive temperature coefficient (TC), and is combined with a V_{BE} voltage having a negative TC to provide the output signal which varies only a little with temperature changes.

Reissue Pat. RE. No. 30,586 (A. P. Brokaw) shows a particularly advantageous band-gap voltage reference requiring only two transistors.

Band-gap reference circuits have primarily been employed in bipolar ICs. Efforts have been made to adapt such references for CMOS ICs, but significant problems have been encountered in those efforts. As a result, the devices proposed for CMOS have suffered important defects, particularly undue complexity.

One serious problem results from the fact that the ΔV_{BE} voltage is quite small (e.g. less than 100 mV), so that it must be amplified quite a bit to reach a value suitable for reference purposes. Such amplification is inherent in a band-gap circuit such as shown in U.S. Pat. RE. No. 30,586 referred to above, because the ΔV_{BE} signal is taken from the collectors of the two transistors. In a CMOS chip made by the usual processes, however, the bipolar transistors available for voltage reference purposes are parasitic transistors, the collectors of which cannot be independently accessed for voltage sensing purposes. In such devices, therefore, the ΔV_{BE} voltage will not automatically be amplified by the transistors from which it is developed.

Moreover, the MOS amplifiers on a CMOS chip have relatively large offset voltages, so that the offset after substantial amplification will show up as a large error compared to the ΔV_{BE} signal component. For example, to develop a reference voltage of around 5 volts, a 20 mV offset in an amplifier (or comparator) could show up as a 0.5 volt error referred to output or threshold.

U.S. Patent 4,622,512 (Brokaw) shows an arrangement for multiplying the V_{BE} of each of two transistors having different current densities by connecting resistor-string V_{BE} multipliers to each of the two transistors. This is an effective approach to the problem, but is not fully satisfactory for all applications.

SUMMARY OF THE INVENTION

In one preferred embodiment of the invention, to be described hereinafter in detail, the voltage reference comprises four pairs of parasitic bipolar transistors with the individual transistors of each pair operated at different current densities. The four low-current-density transistors of these pairs form one sub-set, and are interconnected in a string-like or "stacked" arrangement so that their V_{BE}'s add together cumulatively. The four high-current-density transistors are similarly interconnected as a second sub-set.

End transistors of each string are connected together in such a way as to develop the total cumulative ΔV_{BE} voltage for both strings of transistors. By arranging the transistors of each sub-set to have equal current densities, the net ΔV_{BE} voltage will be four times as large as that obtained with a single pair of transistors operated at such different current densities. Such a large ΔV_{BE} voltage makes possible the development of a stable and precise reference voltage on a CMOS IC chip.

The preferred embodiment to be described further includes MOS transistors interconnected with the parasitic bipolar transistors to provide improved operating characteristics. In a second embodiment of the invention, two (or more) strings of opposite-polarity transistors (e.g., NPN

vs. PNP) are added to the original two strings to further build up the magnitude of the total ΔV_{BE} voltage.

Other objects, aspects and advantages of the invention will in part be pointed out in, and in part apparent from, the following description of the preferred embodiments of the invention, considered together with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a circuit diagram showing, in somewhat simplified form, one preferred embodiment of the invention;

FIGURES 2A and 2B are a more detailed circuit diagram of the embodiment of Figure 1; and

FIGURE 3 is a circuit diagram, in somewhat simplified form, showing an arrangement for further increasing the magnitude of the ΔV_{BE} voltage.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

Referring now to Figure 1, the voltage reference forming part of a CMOS IC chip comprises four pairs of parasitic bipolar PNP transistors Q4, Q5; Q3, Q6; Q2, Q7; and Q1, Q8. The left-hand transistors of these pairs form one sub-set 30 of transistors which, in this embodiment, are all identical. Each transistor of this sub-set is supplied with current from a corresponding current source in the form of a PMOS transistor (M6, M7, M8, M9) having its drain connected to the emitter of the associated bipolar transistor (Q1, Q2, Q3, Q4). These four PMOS current sources are identical, and in this embodiment each furnishes the corresponding bipolar transistor with a current I of one μA.

The right-hand transistors Q5-Q8 of the four transistor pairs form a second sub-set 32 of identical transistors each of which is supplied with a current of 20 μA by a respective PMOS current source M10-M13. The emitter areas of these transistors are one-eighth the emitter areas of the transistors Q1-Q4. Thus, the current density of the transistors in the second sub-set is 160 times the current density of the first sub-set of transistors. For any different-current-density pair of these transistors, the difference in V_{BE} voltages will be:

$$\Delta V_{BE} = \frac{KT}{Q} \ln 160$$

or 0.131 volts.

The bipolar transistors of each of the two sub-sets 30, 32 are interconnected in a string arrangement wherein the emitter of one transistor is connected to the base of the next adjacent transistor. The collectors of all of the transistors are connected to the chip substrate, as indicated by the three-pronged symbol; the substrate is maintained at the negative supply voltage (in this case -5V). With the emitter-to-base string interconnection shown, the V_{BE} voltages of the individual transistors add together cumulatively. By connecting together the bases of the two transistors (Q4, Q5) at a common end of the two strings of transistors, a net cumulative ΔV_{BE} voltage will be developed between circuit points 3 and 4 at the two transistors (Q1, Q8) at the opposite ends of the strings. This net voltage will be four times the ΔV_{BE} voltage for any single pair of the transistors, or about 0.525 volts.

The potentials at circuit points 3 and 4 are connected respectively to the gates of two PMOS transistors M1, M2, which act as a buffer circuit along with M3 and

M4. With this arrangement, the potential at circuit point 4 is effectively transferred to circuit point 2 at the upper end of a resistor R1 in series with the left-hand buffer transistor M1. Thus the voltage across R1 will be the net ΔV_{BE} voltage of (about) 0.525.

The resulting current through R1 is PTAT (proportional to absolute temperature) because it is produced by a ΔV_{BE} voltage. This current is mirrored through M5 to M15 with a ratio producing an M15 current of 250I (i.e., about 250 μA). This latter current flows through a resistor R2, and through a PNP transistor Q9 and series resistors R3, R4. The lower end of resistor R4 is connected to ground, which is the reference terminal for the final output voltage (that is, the ground terminal is midway between the +5V and -5V supply voltages).

The voltage across resistor R2 is, in the preferred embodiment described herein, given by the following expression:

$$V_{R2} = \frac{(\Delta V_{BE})(R2)(250)}{(R1)(80)}$$

In one preferred embodiment R2 = 5.13K, and R1 = 6.565K.

The upper end of resistor R2 is connected to the base of a PNP transistor Q10. This transistor is supplied with current by a PMOS transistor M16, producing a current of 500 I. The emitter of Q10 is connected to the voltage reference output terminal which produces an output voltage V_{OUT} as follows:

$$V_{OUT} = V_{BE}10 + V_{BE}9(1 + X) + \frac{(\Delta V_{BE})(R2)(250)}{(R1)(80)}$$

In the preferred embodiment, R4 was one-half the size of R3, so that X = 0.5

The V_{BE} and ΔV_{BE} terms are so set that the variations in output voltage with changes in temperature are quite small.

The use of buffer transistors M1 through M4 permits a relatively high current to flow in the resistor R1 (i.e., 80 μA as against 1 μA in the PNP transistor Q1). This makes it possible to use a resistor value (about 6.5K) which is practicable to implement. If the 1 μA current of transistor Q1 were arranged to flow through resistor R1, in accordance with prior art concepts, the resistor would have to be about 525 K. A resistor that large would not be manageable in normal processing of an IC chip. The buffer arrangement also allows transistor Q1 to operate at low currents, minimizing Beta effects as well as obtaining high current ratios between individual transistors of each pair without requiring large supply currents.

Figure 2A and 2B present further details of a voltage reference circuit of the type shown in Figure 1. The designations applied to common elements of these two figures remain the same, for ready comparison. It will be seen that the PMOS current sources for the PNP transistors actually comprise two transistors, to provide increased output impedance. It also should be noted that the circuit in Figures 2A and 2B furnishes two separate output voltages to provide for use in two-channel stereo equipment, with minimal cross-talk between channels.

It has been found that still larger ΔV_{BE} voltages can be produced by incorporating further strings of bipolar transistors. Figure 3 shows such an arrangement,

wherein two additional strings 40, 42 of NPN transistors are connected respectively to corresponding upper ends of PNP transistor strings 30, 32 as shown in Figure 1. Because these additional transistors are NPN type, rather than PNP type as in the first two transistor strings, their operating voltages can be cascaded downwardly (starting at the upper ends of the strings) while still increasing cumulatively the net ΔV_{BE} voltage. Approximate voltages at juncture points are shown on the circuit diagram.

As in the Figure 1 circuit, the PNP transistors 30, 32 receive current from PMOS current sources, with the left-hand string transistors receiving 1 μA each and the right-hand PNP transistors receiving 20 μA. The left-hand string emitter areas are eight times that of the right-hand string emitter areas, just as in Figure 1.

The left-hand string of NPN transistors 40 have emitter areas equal to those of the right-hand string of PNP transistors 32 and are supplied with currents of 20 μA by corresponding NMOS current sources. The right-hand string of NPN transistors 42 have emitter areas eight times that of the emitter areas of the left-hand transistor string 40, and are supplied with currents of 1 μA by corresponding NMOS current sources.

The first transistor Q9 of the left-hand NPN string 40 has its base connected to the emitter of the upper end transistor Q7 of the left-hand string of PNP transistors 30. The remaining transistors of this NPN string 40 are interconnected as before, with the emitter of one transistor connected to the base of the next adjacent transistor.

The base of the first transistor Q10 of the right-hand NPN string 42 is connected to the emitter of the upper end transistor Q8 of the right-hand PNP string 32. The remaining transistors of this NPN string are interconnected as before, with the emitter of one transistor being connected to the base of the next adjacent transistor.

With this arrangement, the net ΔV_{BE} voltage can be enlarged by the additive relationship between the four strings of transistors. In one exemplary circuit, a total ΔV_{BE} voltage of 1.04 is shown.

Although preferred embodiments of the invention have been disclosed herein in detail, it is to be understood that this is for the purpose of illustrating the invention, and should not be construed as necessarily limiting the invention since those of skill in this art can readily make various changes and modifications thereto without departing from the scope of the invention as reflected in the claims hereof.

What is Claimed is:

1. In an IC chip formed with a plurality of CMOS transistors together with a plurality of parasitic bipolar transistors having two current-carrying electrodes and a base electrode; a band-gap voltage reference comprising:

a plurality of selected pairs of said bipolar transistors;

said transistor pairs being divided into two sub-sets each comprising one transistor from each pair;

current means supplying to all of the transistors of said selected pairs controlled currents having magnitudes such that the current densities of the individual transistors of each pair are different;

one current-carrying electrode of each of said paired transistors being connected to the base electrode of another transistor of the same sub-set to form inter-connected strings of transistors making up said sub-sets;

means connecting together like electrodes of two common-end transistors of each of said strings of transistors;

first and second MOS transistors connected respectively to the transistors at the ends of said strings of transistors which are opposite said common ends;

resistor means; and

circuit means coupling said first and second MOS transistors to the ends of said resistor means respectively for developing a ΔV_{BE} voltage across said resistor means.

2. A voltage reference as claimed in Claim 1, wherein said bipolar transistors are PNP types; and

means connecting the emitters of the two transistors at said opposite ends of said strings to the gates of said first and second MOS transistors.

3. A voltage reference as claimed in Claim 1, including third and fourth MOS transistors connected respectively in series with said first and second gate-connected MOS transistors to serve as current sources to set the level of current through said first and second MOS transistors.

4. In an IC chip formed with a plurality of CMOS transistors together with a plurality of parasitic bipolar transistors having two current-carrying electrodes and a base electrode; a band-gap voltage reference comprising:

a plurality of selected pairs of said bipolar transistors;

said transistor pairs being divided into two sub-sets each comprising one transistor from each pair;

the emitter areas of said first sub-set transistors being substantially different from the emitter areas of said second sub-set transistors;

first current means supplying to all of the transistors of said first sub-set controlled currents of predetermined magnitudes;

second current means supplying to all of the transistors of said second sub-set controlled currents of magnitudes substantially different from the current magnitudes of said first sub-set transistors and having such magnitudes that the current densities of the individual transistors of each pair are different;

one current-carrying electrode of each of said paired transistors being connected to the base electrode of another transistor of the same sub-set to form interconnected strings of transistors making up said sub-sets;

means connecting together like electrodes of two common-end transistors of each of said strings of transistors; and

circuit means connected to the transistors at the ends of said strings of transistors which are opposite sad common ends for developing a ΔV_{BE} voltage.

5. A voltage reference as claimed in claim 4, wherein the emitter areas of said first sub-set transistors are larger than the emitter areas of said second sub-set transistors; and

the currents supplied to said first sub-set transistors are smaller than the currents supplied to said second sub-set transistors;

whereby the current densities of said first sub-set transistors are made substantially smaller than the current densities of said second sub-set transistors, both by the emitter area differentials and by the current differentials.

6. In an IC chip formed with a plurality of bipolar transistors having two current-carrying electrodes and a base electrode; a band-gap voltage reference comprising:

a first set of pairs of said bipolar transistors of one polarity;

said first set of pairs being divided into first and second sub-sets each comprising one transistor from each pair;

first current means supplying to all of the transistors of said first set of pairs controlled currents having magnitudes such that the current densities of the individual transistors of each pair are different;

emitter electrodes of the transistors of said first and second sub-sets being connected to respective base electrodes of adjacent transistors of the same sub-set to form first and second interconnected strings of transistors making up said first and second sub-sets respectively;

means connecting together like electrodes of two common-end transistors of each of said first and second strings of transistors;

a second set of pairs of said bipolar transistors of polarity opposite said one polarity;

said second set of pairs being divided into third and fourth sub-sets each comprising one transistor from each pair;

second current means supplying to all of the transistors of said second set of pairs controlled currents having magnitudes such that the current densities of the individual transistors of each pair are different;

emitter electrodes of the transistors of said third and fourth sub-sets being connected to respective base electrodes of adjacent transistors of the same sub-set to form third and fourth interconnected strings of transistors making up said third and fourth sub-sets;

means connecting the ends of said first and second strings which are opposite said common end to corresponding ends of said third and fourth strings of transistors; and

circuit means connected to the two transistors at the ends of said third and fourth strings of transistors which are opposite said corresponding ends for developing a ΔV_{BE} voltage.

7. A voltage reference as claimed in Claim 6, wherein said current means comprise MOS current source transistors having the same polarity as the bipolar transistors for which they supply current.

8. A voltage reference as claimed in Claim 7, wherein said first and second strings of transistors are PNP type;

said current sources for said first and second strings of transistors comprising PMOS transistors.

AMENDED CLAIMS
[received by the International Bureau on 11 February 1992 (11.02.92); original claim 3 amended; other claims unchanged (1 page)]

3. A voltage reference as claimed in Claim 1, including third and fourth MOS transistors connected respectively in series with said first and second MOS transistors to serve as a current mirror to force the currents through said first and second MOS transistors to be the same.

4. In an IC chip formed with a plurality of CMOS transistors together with a plurality of parasitic bipolar transistors having two current-carrying electrodes and a base electrode; a band-gap voltage reference comprising:

a plurality of selected pairs of said bipolar transistors;

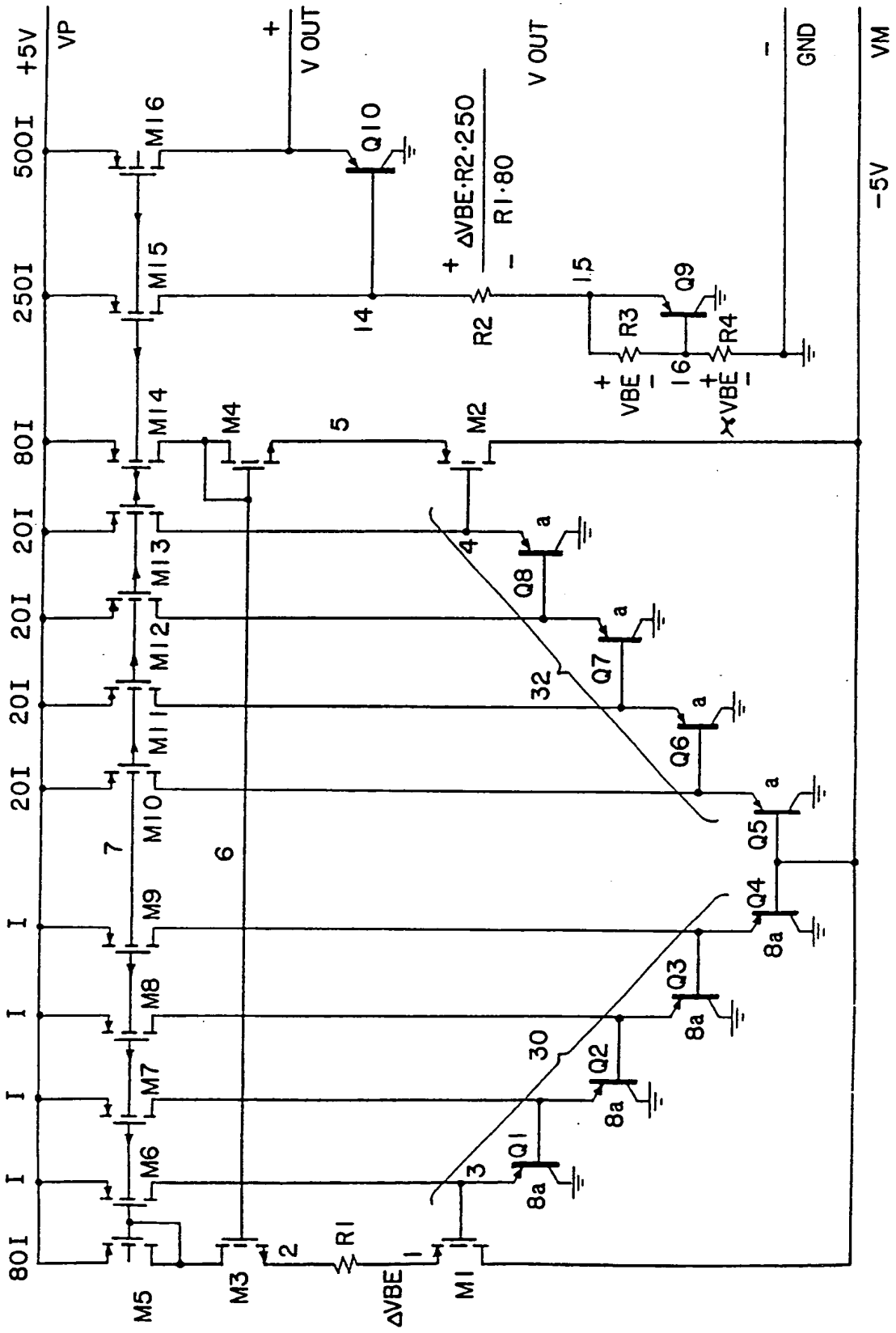
said transistor pairs being divided into two sub-sets each comprising one transistor from each pair;

the emitter areas of said first sub-set transistors being substantially different from the emitter areas of said second sub-set transistors;

first current means supplying to all of the transistors of said first sub-set controlled currents of predetermined magnitudes;

second current means supplying to all of the transistors of said second sub-set controlled currents of magnitudes substantially different from the current magnitudes of said first sub-set transistors and having such magnitudes that the current densities of the individual transistors of each pair are different;

one current-carrying electrode of each of said paired transistors being connected to the base electrode of another transistor of the same sub-set to form interconnected strings of transistors making up said sub-sets;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M14
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20I
M11
20I
M10
20I
7
6
M9
I
M8
I
M7
I
M6
I
80I
M5
M3
2
R1
ΔVBE
1
M1
4
Q8
a
32
Q7
Q6
Q5
Q4
8a
Q3
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Q2
Q1
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+ ΔVBE·R2·250
– R1·80
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Q9
R3
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R4
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+ VBE –
–
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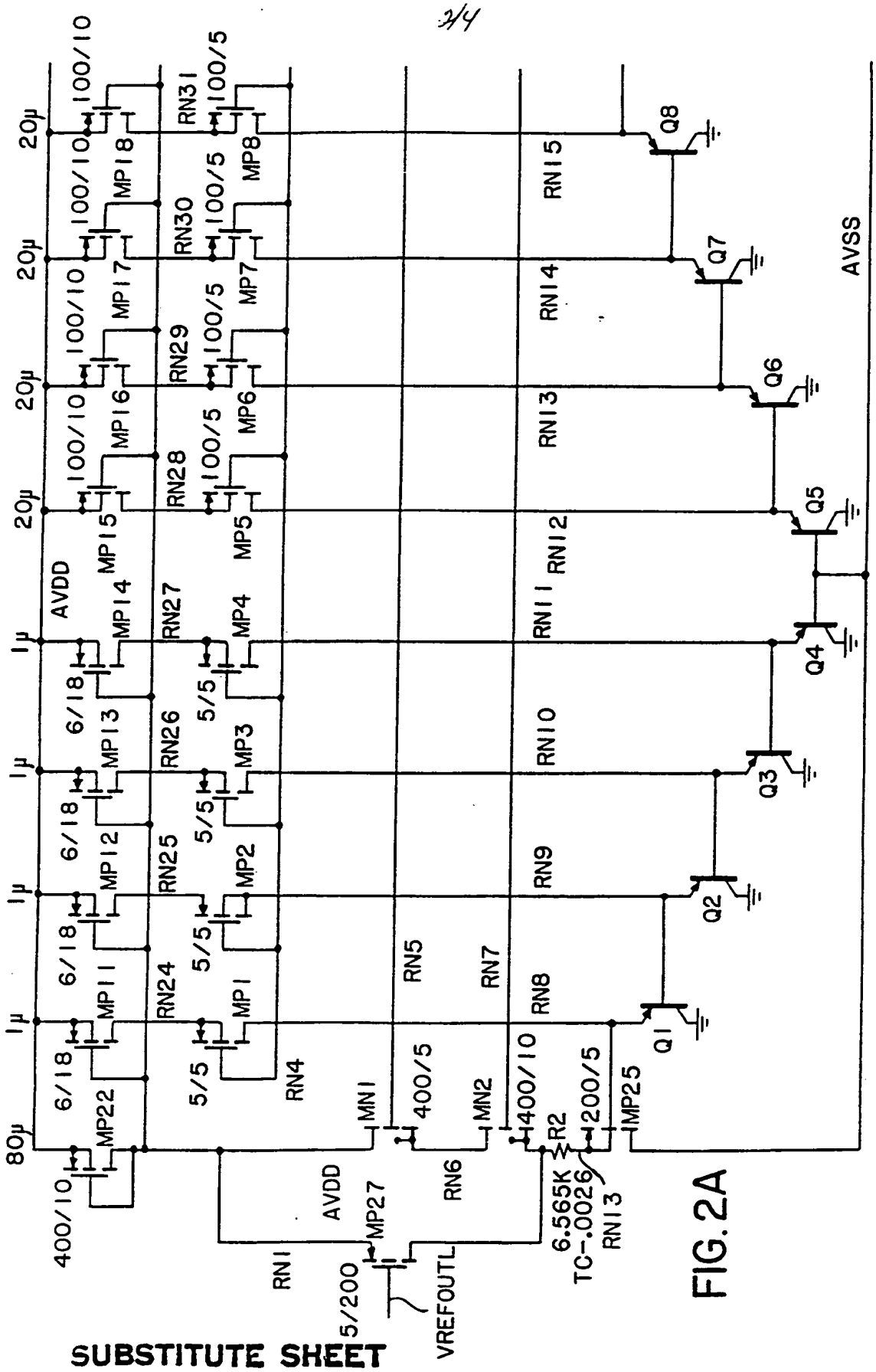
FIG. 1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MP18
MP22
MP25
MP27
MN1
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Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
R2
80µ
20µ
1µ
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100/5
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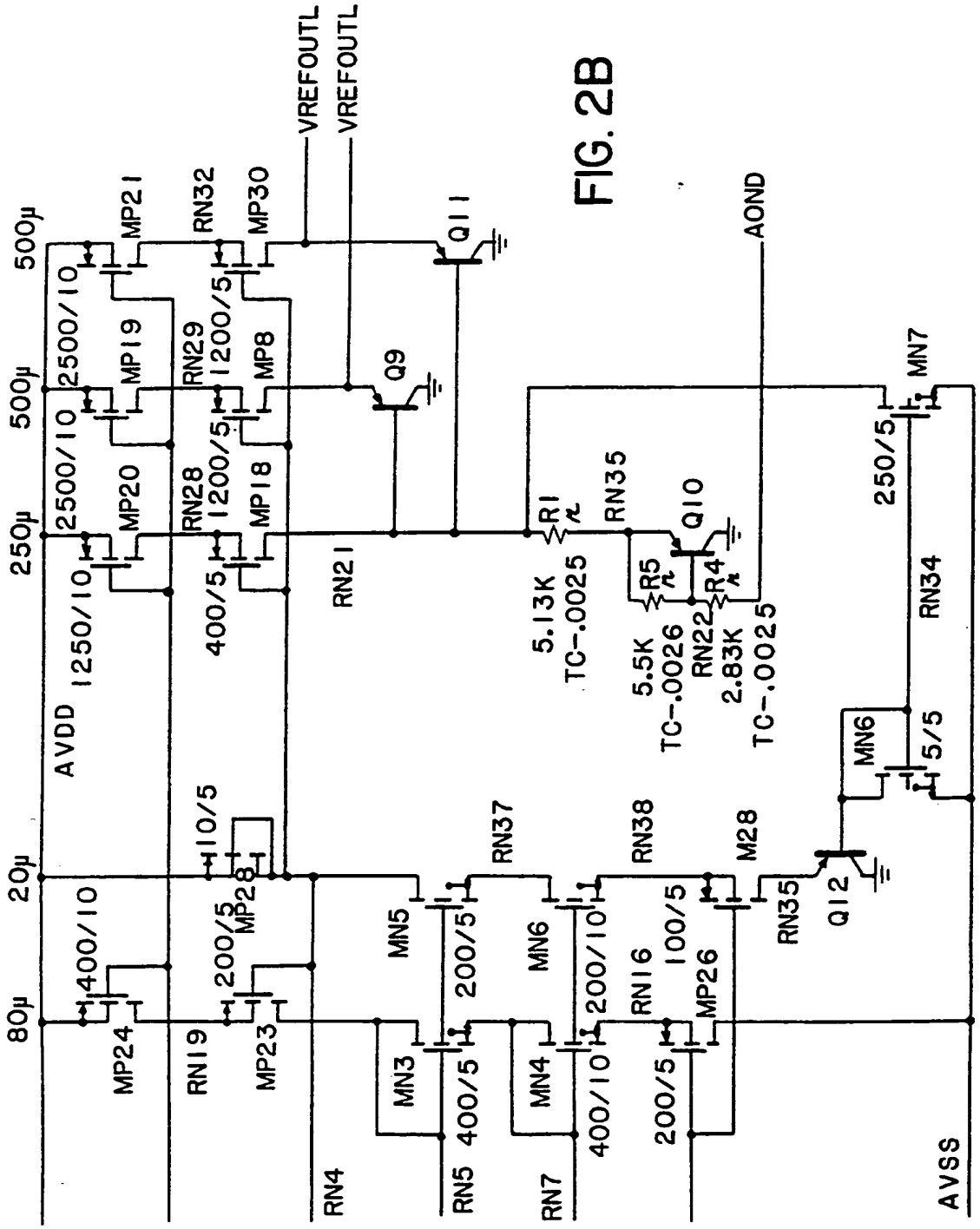
FIG. 2A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RN16
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M28
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Q12
MN7
RN34
MN6
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RN35
Q10
R5
R4
RN22
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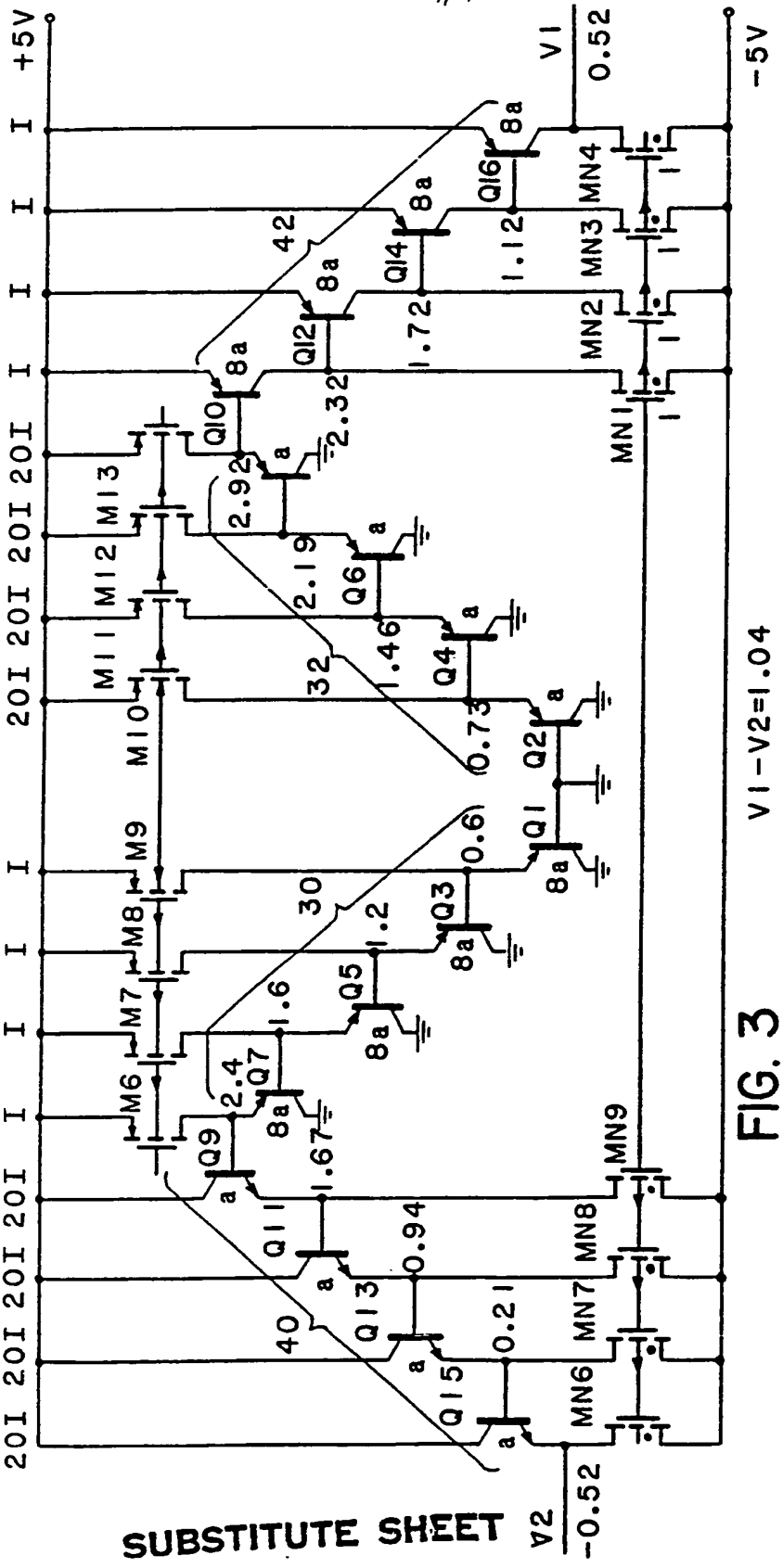
TC-.0025

FIG. 2B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-5V
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V2
-0.52
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Q10 Q12 Q14 Q16
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q9 Q11 Q13 Q15
MN1 MN2 MN3 MN4 MN6 MN7 MN8 MN9
8a
a
2.32
1.72
1.12
2.92
2.19
1.46
0.73
0.6
1.2
1.6
2.4
1.67
0.94
0.21
42
32
30
40

FIG. 3

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US91/06939

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC (5): G05F 3/24

U.S.Cl.: 323/313,314; 307/296.1,296.8; 365/189.09

II FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
U.S.	323/312-316; 307/296.1,296.5-296.8; 365/189.09

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III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	US, A, 4,896,094 (GREAVES ET AL.) 23 January 1990 See entire document	1-11

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
02 December 1991	15 JAN 1992
International Searching Authority	**Signature of Authorized Officer**
ISA/US	Emanuel Todd Voeltz

Form PCT/ISA/210 (second sheet) (Rev.11-87)